

# CBCS SCHEME



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15EC46

## Fourth Semester B.E. Degree Examination, June/July 2019 Linear Integrated Circuits

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

### Module-1

- 1 a. With a neat circuit diagram. Explain the basic op-amp circuit. (06 Marks)
- b. Define the following parameters and mention their typical values for op-amp 741.  
i) Common Mode Rejection Ratio (CMRR) ii) Slew Rate iii) input offset voltage. (06 Marks)
- c. A 741 op-amp is used in a non inverting amplifier with a voltage gain of 50. Calculate the typical output voltage that would result from a common mode input with a peak level of 100mV. (04 Marks)

OR

- 2 a. Sketch the circuit of a three input non inverting summing amplifier. Explain the operation of the circuit and derive an equation for the output voltage. (07 Marks)
- b. With a neat circuit diagram, explain direct coupled non -inverting amplifier with necessary design steps. (05 Marks)
- c. Design an inverting amplifier using LF353 BIFET op-amp. The voltage gain is to be 50 and. The output voltage amplitude is to be 2.5V. (04 Marks)

### Module-2

- 3 a. With a neat circuit diagram, explain the design steps for :  
i) capacitor coupled voltage follower ii) capacitor coupled inverting amplifier. (10 Marks)
- b. Explain how the upper cutoff frequency can be set for inverting and non inverting amplifiers. (06 Marks)

OR

- 4 a. Draw the circuit of a precision voltage source using an op-amp and a zener diode. Explain the circuit operation. (06 Marks)
- b. Draw the complete circuit of an instrumentation amplifier and explain its operation. (06 Marks)
- c. What are the advantages of precision rectifier over simple diode rectifier? (04 Marks)

### Module-3

- 5 a. Draw the circuit of an op-amp precision clamping circuit and explain its operation with necessary design steps. (08 Marks)
- b. With a neat circuit diagram and waveforms, explain the operations of op-amp sample and hold circuit. (08 Marks)

OR

- 6 a. Using a 741 op-amp with a supply of  $\pm 12V$ , design a phase shift oscillator to have an output frequency of 3.5 KHz. (06 Marks)
- b. With a neat circuit diagram and waveforms, explain the operation of differentiating circuit using op-amp. (04 Marks)
- c. With a neat circuit, explain the operation of a fundamental log amplifier using op-amp. Derive the output voltage equation. (06 Marks)

1 of 2

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
2. Any revealing of identification, appeal to evaluator and /or equations written eg.  $42+8 = 50$ , will be treated as malpractice.

**Module-4**

- 7 a. What do you mean by active filter? Explain how active filters are classified. (04 Marks)  
b. Design a first order active low pass filter to have a cutoff frequency of 1KHz. Use 741 op-amp. (05 Marks)  
c. Draw the circuit of a second order active high pass filter and explain its working. (07 Marks)

**OR**

- 8 a. What is voltage regulator? With a neat circuit explain the working of series op-amp regulator. (05 Marks)  
b. Define the following performance parameters of a voltage regulators i) line regulation (04 Marks)  
ii) load regulation. (04 Marks)  
c. With a neat functional diagram, explain the operation of low voltage regulator using IC 723. (07 Marks)

**Module-5**

- 9 a. Draw the block diagram representation of Phase Locked Loop (PLL) and explain its operation. (06 Marks)  
b. Define lock in range and capture range with reference to Phase Locked Loop (PLL). (04 Marks)  
c. With a neat sketch, explain the working of R-2R ladder digital to analog convertor (DAC). (06 Marks)

**OR**

- 10 a. Draw and explain the functional diagram of 555 timer. (06 Marks)  
b. With a neat sketch and waveforms explain the working of astable multivibrator using 555 timer. (06 Marks)  
c. Design a monostable multi vibrator using 555 timer to obtain a pulse width of 5 msec. (04 Marks)

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